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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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APPLIED MATERIALS, INC.
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EXAMINER
PERALTA, GINETTE

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/052,681	Applicant(s) XI ET AL.	
	Examiner Ginette Peralta	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-38 in Paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,2, 9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Taguchi et al. (U. S. Pat. 5,308,793).

Regarding claim 1, Taguchi et al. discloses, in col. 5, ll. 4-30, a method of filling a via in a patterned substrate that comprises depositing a generally conformal first barrier layer 3 on the patterned substrate by chemical vapor deposition (col. 5, l. 6); removing the first barrier layer from the horizontal surfaces of the patterned substrate (col. 5, ll. 16-19); depositing a second barrier layer 4 by physical vapor deposition(col. 5, ll. 31-34); and then depositing a conductive material 5 (col. 5, ll. 39-41).

Regarding claim 2, Taguchi et al. discloses depositing a seed layer and a metal layer in the via after the second barrier layer is deposited by a two-stage deposition process (col. 5, ll. 39-63).

Regarding claim 9, Taguchi et al. discloses depositing the seed layer by physical vapor deposition.

Regarding claim 12, Taguchi et al. discloses the metal layer deposited by physical vapor deposition.

Regarding claim 15, Taguchi et al. discloses that the method is applied to structures having a high aspect ratio (col. 3, ll. 36-41), aspect ratios exceeding one, and that the invention is an improvement on teachings of filling holes having aspect ratios of 4 (col. 1, ll. 36-64).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. in view of Zhao et al. (U. S. Pat. 5,674,787).

Regarding claim 3, Taguchi et al. discloses the first barrier layer comprising silicon nitride. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use silicon nitride as Taguchi et al. teaches or any other suitable barrier material that is well known in the art for the disclosed intended purpose of providing a fine quality barrier, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Regarding claim 4, Taguchi et al. discloses the second barrier layer comprising titanium or titanium nitride.

Taguchi et al. teaches the claimed invention with the exception of the second barrier layer selected from tantalum, tantalum nitride, titanium silicon nitride, tantalum silicon nitride, tungsten and tungsten nitride.

Zhao et al. discloses a method of filling a via in a patterned substrate that comprises depositing a barrier layer; and depositing a conductive material; wherein the barrier layer is selected from titanium nitride, tantalum, tantalum nitride or tungsten nitride, wherein these materials are used for the disclosed intended purpose of serving as an anti-reflection coating layer as well as an electromigration and/or stress migration suppression layer for the via conductive material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a barrier layer of titanium nitride as both Taguchi et al. and Zhao et al. or to use a barrier layer of any of the materials taught by Zhao et al.

disclose in order to reduce the electromigration of copper, which is a well-known result of the absence of a barrier layer. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use any of the barrier layer materials taught by Zhao et al. in the invention of Taguchi et al. or any other suitable barrier material that is well known in the art for the disclosed intended purpose of providing an electromigration and/or stress migration suppression layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Regarding claim 16, Taguchi et al. discloses that the second barrier layer has a thickness of 0.1μ. Thus, Taguchi et al. discloses the claimed invention except for teaching a thickness of 20Å to about 50Å. It would have been an obvious matter of design choice to adjust the thickness of the barrier layer in accordance to the size of the via in which the barrier layer is formed, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1955).*

Regarding claim 17, Taguchi et al. discloses the second barrier layer comprising titanium or titanium nitride. Taguchi et al. teaches the claimed invention with the exception of the second barrier layer selected from tantalum, tantalum nitride, titanium silicon nitride, tantalum silicon nitride, tungsten and tungsten nitride.

Zhao et al. discloses a method of filling a via in a patterned substrate that comprises depositing a barrier layer; and depositing a conductive material; wherein the barrier layer is selected from titanium nitride, tantalum, tantalum nitride or tungsten nitride, wherein these materials are used for the disclosed intended purpose of serving as an anti-reflection coating layer as well as an electromigration and/or stress migration suppression layer for the via conductive material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a barrier layer of titanium nitride as both Taguchi et al. and Zhao et al. or to use a barrier layer of any of the materials taught by Zhao et al. disclose in order to reduce the electromigration of copper, which is a well-known result of the absence of a barrier layer. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use any of the barrier layer materials taught by Zhao et al. in the invention of Taguchi et al. or any other suitable barrier material that is well known in the art for the disclosed intended purpose of providing an electromigration and/or stress migration suppression layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Furthermore, Taguchi et al. discloses that the second barrier layer has a thickness of 0.1μ. Thus, Taguchi et al. discloses the claimed invention except for teaching a thickness of 20Å to about 50Å. It would have been an obvious matter of design choice to

adjust the thickness of the barrier layer in accordance to the size of the via in which the barrier layer is formed, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1955).*

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. in view of Zhao et al. as applied to claims 3, 4, and 16, 17 above, and further in view of Simon et al. (U. S. Pat. 5,933,753).

Taguchi et al. as modified by Zhao et al. discloses that the metal layer is aluminum or copper, furthermore, as modified by Zhao et al., it would have been obvious to one of ordinary skill in the art to use copper instead of aluminum as Zhao et al. teaches the use of copper preferably over aluminum because copper has better electromigration properties and a lower resistivity. Thus, Taguchi et al. as modified by Zhao et al. discloses the claimed invention with the exception of the seed layer being copper.

Simon et al. discloses a method of filling a via that comprises forming a seed layer of copper prior to the deposition of the metal layer of copper, the seed layer being copper for the disclosed intended purpose of creating an environment that is more conducive to a deposition of copper, and facilitating the formation of a single crystalline copper structure at the via-metal interface.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a seed layer of copper on which to deposit the copper

metal layer, for the disclosed intended purpose of creating an environment that is more conducive to a deposition of copper, and facilitating the formation of a single crystalline copper structure at the via-metal interface.

7. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. in view of Zhao et al. (U. S. Pat. 5,846,332).

Taguchi et al. discloses, in col. 5, ll. 4-30, a method of filling a via in a patterned substrate that comprises depositing a generally conformal first barrier layer 3 on the patterned substrate by chemical vapor deposition (col. 5, l. 6); removing the first barrier layer from the horizontal surfaces of the patterned substrate (col. 5, ll. 16-19); depositing a second barrier layer 4 by physical vapor deposition (col. 5, ll. 31-34); and then depositing a conductive material 5 (col. 5, ll. 39-41).

Taguchi et al. discloses the claimed invention with the exception of the first barrier layer being deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool.

Zhao et al. discloses a substrate processing chamber, particularly a chemical vapor deposition chamber used for both a thermal deposition and a subsequently performed plasma process, wherein the single chamber is proposed for the disclosed intended purpose of extending the mean number of wafers between cleans by improving the performance of the semiconductor substrate processing chamber. Zhao et al. further discloses that other typical plasma processes can be performed in the chamber.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a single processing chamber as the one taught by Zhao et al. for the disclosed intended purpose of Zhao et al. of extending the mean number of wafers between cleans by improving the performance of the substrate processing chamber.

8. Claims 10, and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. in view of Gelatos et al. (U. S. Pat. 5,391,517).

Taguchi et al. discloses the claimed invention including the deposition of the metal layer and the seed layer by physical vapor deposition, and with the exception of disclosing alternate methods of deposition.

Gelatos et al. discloses in col. 5, ll. 14-20, that copper can be deposited by conventional chemical vapor deposition, plasma assisted chemical vapor deposition, plasma-enhanced chemical vapor deposition, sputter deposition (i.e. physical vapor deposition), electroplating, and the like, wherein these deposition processes can be used as an alternative.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the copper layer and the copper seed layer by any of chemical vapor deposition, physical vapor deposition, electroplating, and other conventionally known and used deposition processes, in order to deposit copper in the structure.

9. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uzoh (U. S. Pat. 5,930,669).

Uzoh discloses a method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, the method comprising depositing a generally conformal first barrier layer 30 on the patterned substrate by physical vapor deposition; depositing a conductive material.

Uzoh discloses the claimed invention with the exception of forming the barrier layer by chemical vapor deposition, removing the first barrier layer from the horizontal surface of the patterned substrate, and depositing by physical vapor deposition a second barrier layer.

Taguchi et al. discloses, in col. 5, ll. 4-30, a method of filling a via in a patterned substrate that comprises depositing a generally conformal first barrier layer 3 on the patterned substrate by chemical vapor deposition (col. 5, l. 6); removing the first barrier layer from the horizontal surfaces of the patterned substrate (col. 5, ll. 16-19); depositing a second barrier layer 4 by physical vapor deposition(col. 5, ll. 31-34); and then depositing a conductive material 5 (col. 5, ll. 39-41), wherein the first barrier layer is removed from the horizontal surfaces of the patterned substrate and a second barrier layer is formed for the disclosed intended purpose of preventing the oxidation of the barrier metal and completely burying connection holes which have a high aspect ratio which exhibit desirably low resistance characteristics.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the first barrier layer from the horizontal surfaces, and to deposit a second barrier layer for the disclosed intended purpose of preventing the oxidation of the barrier metal and completely burying connection holes which have a high aspect ratio which exhibit desirably low resistance characteristics.

10. Claims 18 –21, 26, 29, 32-34, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (U. S. Pat. 5,308,793) in view of Zhao et al. (U. S. Pat. 5,674,787) and Emesh (U. S. Pat. 5,407,698).

Regarding claims 8, 20, 21 and 38, Taguchi et al. discloses, in col. 5, ll. 4-30, a method of filling a via in a patterned substrate that comprises depositing a generally conformal first barrier layer 3 on the patterned substrate by chemical vapor deposition (col. 5, l. 6); removing the first barrier layer from the horizontal surfaces of the patterned substrate (col. 5, ll. 16-19); depositing a second barrier layer 4 by physical vapor deposition(col. 5, ll. 31-34); and then depositing a conductive material 5 (col. 5, ll. 39-41).

Taguchi et al. discloses the claimed invention with the exception of the first barrier layer being formed by atomic layer deposition, and the first barrier layer comprising one of tantalum, tantalum nitride, tungsten, and tungsten nitride

Zhao et al. discloses a method of filling a via in a patterned substrate that comprises depositing a barrier layer; and depositing a conductive material; wherein the barrier layer is selected from titanium nitride, tantalum, tantalum nitride or tungsten nitride, wherein these materials are used for the disclosed intended purpose of serving

as an anti-reflection coating layer as well as an electromigration and/or stress migration suppression layer for the via conductive material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a barrier layer of titanium nitride as both Taguchi et al. and Zhao et al. or to use a barrier layer of any of the materials taught by Zhao et al. disclose in order to reduce the electromigration of copper, which is a well-known result of the absence of a barrier layer. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use any of the barrier layer materials taught by Zhao et al. in the invention of Taguchi et al. or any other suitable barrier material that is well known in the art for the disclosed intended purpose of providing an electromigration and/or stress migration suppression layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Emesh discloses forming a film comprising tungsten by atomic layer deposition on a semiconductor substrate, wherein the method of deposition is atomic layer deposition for the disclosed intended purpose of depositing a layer having a high step coverage, and a smooth surface, which is desired in highly integrated devices due to the subsequent levels that will bi formed in the substrate.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use atomic layer deposition instead of chemical vapor

deposition for the disclosed intended purpose of depositing a layer having a high step coverage, and a smooth surface, which is desired in highly integrated devices due to the subsequent levels that will bi formed in the substrate.

Regarding claim 19, Taguchi et al. discloses depositing a seed layer and a metal layer in the via after the second barrier layer is deposited by a two-stage deposition process (col. 5, ll. 39-63).

Regarding claim 26, Taguchi et al. discloses depositing the seed layer by physical vapor deposition.

Regarding claim 29, Taguchi et al. discloses the metal layer deposited by physical vapor deposition.

Regarding claim 32, Taguchi et al. discloses that the method is applied to structures having a high aspect ratio (col. 3, ll. 36-41), aspect ratios exceeding one, and that the invention is an improvement on teachings of filling holes having aspect ratios of 4 (col. 1, ll. 36-64).

Regarding claim 33, Taguchi et al. discloses that the second barrier layer has a thickness of 0.1μ. Thus, Taguchi et al. discloses the claimed invention except for teaching a thickness of 20Å to about 50Å. It would have been an obvious matter of design choice to adjust the thickness of the barrier layer in accordance to the size of the via in which the barrier layer is formed, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1955).*

Regarding claim 34, Taguchi et al. discloses the second barrier layer comprising titanium or titanium nitride. Taguchi et al. teaches the claimed invention with the exception of the second barrier layer selected from tantalum, tantalum nitride, titanium silicon nitride, tantalum silicon nitride, tungsten and tungsten nitride.

Zhao et al. discloses a method of filling a via in a patterned substrate that comprises depositing a barrier layer; and depositing a conductive material; wherein the barrier layer is selected from titanium nitride, tantalum, tantalum nitride or tungsten nitride, wherein these materials are used for the disclosed intended purpose of serving as an anti-reflection coating layer as well as an electromigration and/or stress migration suppression layer for the via conductive material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a barrier layer of titanium nitride as both Taguchi et al. and Zhao et al. or to use a barrier layer of any of the materials taught by Zhao et al. disclose in order to reduce the electromigration of copper, which is a well-known result of the absence of a barrier layer. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use any of the barrier layer materials taught by Zhao et al. in the invention of Taguchi et al. or any other suitable barrier material that is well known in the art for the disclosed intended purpose of providing an electromigration and/or stress migration suppression layer, since it has been held to be within the general skill of a worker in the art to select a

known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Furthermore, Taguchi et al. discloses that the second barrier layer has a thickness of 0.1μ. Thus, Taguchi et al. discloses the claimed invention except for teaching a thickness of 20Å to about 50Å. It would have been an obvious matter of design choice to adjust the thickness of the barrier layer in accordance to the size of the via in which the barrier layer is formed, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1955).*

11. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. in view of Zhao et al. and Emesh as applied to claims 18-21 above, and further in view of Simon et al..

Taguchi et al. as modified by Zhao et al. discloses that the metal layer is aluminum or copper, furthermore, as modified by Zhao et al., it would have been obvious to one of ordinary skill in the art to use copper instead of aluminum as Zhao et al. teaches the use of copper preferably over aluminum because copper has better electromigration properties and a lower resistivity. Thus, Taguchi et al. as modified by Zhao et al. discloses the claimed invention with the exception of the seed layer being copper.

Simon et al. discloses a method of filling a via that comprises forming a seed layer of copper prior to the deposition of the metal layer of copper, the seed layer being

copper for the disclosed intended purpose of creating an environment that is more conducive to a deposition of copper, and facilitating the formation of a single crystalline copper structure at the via-metal interface.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a seed layer of copper on which to deposit the copper metal layer, for the disclosed intended purpose of creating an environment that is more conducive to a deposition of copper, and facilitating the formation of a single crystalline copper structure at the via-metal interface.

12. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (U. S. Pat. 5,308,793) in view of Zhao et al. (U. S. Pat. 5,674,787) and Emesh (U. S. Pat. 5,407,698) as applied to claims 18-21 above, and further in view of Zhao et al. (U. S. Pat. 5,846,332).

Taguchi et al., as modified by Zhao et al. ('787) and Emesh, discloses, in col. 5, ll. 4-30, a method of filling a via in a patterned substrate that comprises depositing a generally conformal first barrier layer 3 on the patterned substrate by chemical vapor deposition (col. 5, l. 6); removing the first barrier layer from the horizontal surfaces of the patterned substrate (col. 5, ll. 16-19); depositing a second barrier layer 4 by physical vapor deposition (col. 5, ll. 31-34); and then depositing a conductive material 5 (col. 5, ll. 39-41).

Taguchi et al. discloses the claimed invention with the exception of the first barrier layer being deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool.

Zhao et al. ('332) discloses a substrate processing chamber, particularly a chemical vapor deposition chamber used for both a thermal deposition and a subsequently performed plasma process, wherein the single chamber is proposed for the disclosed intended purpose of extending the mean number of wafers between cleans by improving the performance of the semiconductor substrate processing chamber. Zhao et al. further discloses that other typical plasma processes can be performed in the chamber.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a single processing chamber as the one taught by Zhao et al. for the disclosed intended purpose of Zhao et al. of extending the mean number of wafers between cleans by improving the performance of the substrate processing chamber.

13. Claims 27-28, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (U. S. Pat. 5,308,793) in view of Zhao et al. (U. S. Pat. 5,674,787) and Emesh (U. S. Pat. 5,407,698) as applied to claims 18-21, 26 and 29 above, and further in view of Gelatos et al..

Taguchi et al., as modified by Zhao et al. and Emesh, discloses the claimed invention including the deposition of the metal layer and the seed layer by physical vapor deposition, and with the exception of disclosing alternate methods of deposition.

Gelatos et al. discloses in col. 5, ll. 14-20, that copper can be deposited by conventional chemical vapor deposition, plasma assisted chemical vapor deposition, plasma-enhanced chemical vapor deposition, sputter deposition (i.e. physical vapor deposition), electroplating, and the like, wherein these deposition processes can be used as an alternative.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the copper layer and the copper seed layer by any of chemical vapor deposition, physical vapor deposition, electroplating, and other conventionally known and used deposition processes, in order to deposit copper in the structure.

14. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. in view of Cronin (U. S. Pat. 5,818,110).

Taguchi et al. discloses in col. 5, ll. 4-30, a method of filling a via in a patterned substrate that comprises depositing a generally conformal first barrier layer 3 on the patterned substrate by chemical vapor deposition (col. 5, l. 6); removing the first barrier layer from the horizontal surfaces of the patterned substrate (col. 5, ll. 16-19); depositing a second barrier layer 4 by physical vapor deposition(col. 5, ll. 31-34); and then depositing a conductive material 5 (col. 5, ll. 39-41).

Taguchi et al. discloses the claimed invention with the exception of having an etch stop layer and removing the etch stop layer.

Cronin discloses in fig. 12 and col. 6, ll. 10-34 a method of forming a via that comprises forming a first barrier layer 36 over a patterned layer, the patterned layer comprising an etch stop, removing the first barrier layer from the horizontal surfaces of the patterned substrate (col. 6, ll. 19-24); and removing the etch stop 30 from the bottom of the via wherein an etch stop is used and removed for the disclosed intended purpose of protecting the underlying metal and exposing the metal line in order to allow an electrical connection after the first barrier layer is deposited and removed.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an etch stop layer underlying the first barrier layer in order to protect the underlying conductive region in the invention of Taguchi et al. as Cronin teaches, and to remove it in order to allow an electrical connection to the conductive region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

GP
June 16, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800